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(54) Title: SAMPLE AND HOLD COLUMN BUFFER FOR REFLECTIVE LCD

(57) Abstract: A system for generating an image in a reflective LCD (RLCD) using pulsed current sources instead of pulsed voltage sources to reduce noise and power consumption. The current is provided by a plurality of RAM-driven integrating DACs (IDAC) having a current output. Each IDAC drives one or more of a plurality of RLCD columns in conjunction with one of a plurality of operational transconductance amplifiers (OTA). Time-integration of the applied current by the intrinsic column capacitance of the RLCD creates a controlled voltage ramp on the column capacitance. A Look-Up-Table within each RAM holds a plurality of 8-bit digital values that correspond to the time-derivative of the current values.

SAMPLE AND HOLD COLUMN BUFFER FOR REFLECTIVE LCD

The invention relates to an image processing system as is specified in the precharacterizing part of Claim 1.

The invention further relates to a reflective LCD (RLCD) as is specified in claim 13.

The invention further relates to a method for generating an image in an RLCD.

In a RLCD having a matrix of m horizontal rows and n vertical columns, each m-n intersection forms a cell or picture element (pixel). By applying an electric potential difference, such as 7.5 volts (v), across a cell, a phase change occurs in the crystalline structure at the cell site causing the pixel to change the incident light polarization vector orientation, thereby blocking the light from emerging from the electro-optical system. Removing the voltage across the pixel causes the liquid crystal in the pixel structure to return to the initial "bright" state. Variations in the applied voltage level produce a plurality of different gray shades between the light and dark limits.

The load that an RLCD presents to a driving circuit is best represented as the sum of the individual pixel capacitances and column line, which can be 12 picofarads (pF) for an individual column of an RLCD having 1024 rows. This load becomes 7.68 nanofarads (ηF) for a group of 640 such columns.

At the individual columns, a comparator and a track-and-hold transfer gate are employed to instantaneously terminate the individual column voltage rise when the column capacitance has charged to a predetermined voltage level needed to produce a particular grayscale. As each column terminates at a unique level along the global voltage ramp, a separate pulse-length modulating signal is produced for each individual column.

At the end of a predetermined row time interval, the column voltages are discharged to a fixed reference voltage and the procedure is repeated for the next row. During discharge, a high instantaneous current spike may occur. Assuming all 1024 rows are charged at 7.5 v, a current discharge in approximately 30 nanoseconds (ηs) will generate a peak current of approximately 2 amperes (A). This process is repeated for all the m rows of the

LCD to complete a single frame. Repetition of the frame activity allows for the continual updating of the displayed information with refresh rates typically being 60 Hz for video displays. To better appreciate the above process, it would be beneficial to review U.S. Patent No. 4,766,430 to Gillette et al. which is incorporated herein by reference.

A principal drawback of conventional high current switching circuits of the type just described is that any high speed voltage changes applied to the capacitive load of the RLCD produces very high instantaneous current spikes, i.e., 2 amperes, which in turn produce charge coupling errors within adjacent pixels. In addition, such high current switching devices are not easily configurable within an integrated circuit.

Thus, there is a demonstrated need for an improvement of existing voltage-driven RLCD column driver circuits which would reduce the instantaneous column switching currents and the associated crosstalk interference.

It is an object of the invention to provide an image processing system having reduced instantaneous column switching currents and associated crosstalk interference.

This object is achieved by the image processing system according to the invention as specified in Claim 1.

A system for generating an image in an RLCD from an Integrating Digital-to-Analog Converter (IDAC) that outputs a current pulse rather than a voltage pulse. The IDAC output in series with a plurality of low-current operational transconductance amplifiers (OTAs) is integrated and filtered by the intrinsic capacitance of the RLCD columns thereby reducing noise and power consumption. The IDAC is driven by a Look-Up-Table (LUT) within a Random Access Memory (RAM), which is used to store eight bit time-derivative digital values of the drive currents.

Further advantageous embodiments of the image processing system according to the invention are specified in the dependent claims.

It is a further object of the invention to provide an RLCD having reduced instantaneous column switching currents and associated crosstalk interference.

This object is achieved by the RLCD according to the invention as specified in Claim 13.

Further advantageous embodiments of the RLCD according to the invention are specified in the dependent claims.

It is a further object of the invention to provide a method for generating an image in an RLCD having reduced instantaneous column switching currents and associated crosstalk interference.

This object is achieved by the method for generating an image in an RLCD according to the invention as specified in claim 17.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawing:

Figure 1 shows a conventional control circuit for generating an analog excitation voltage,

Figure 2 shows an exemplary embodiment of a control circuit for an analog current excitation path of an RLCD column fabricated according to the present invention, and

Figure 3 shows representative waveforms of the voltage applied to the RLCD columns of the present invention.

Figure 1 shows a conventional control circuit 10 for generating the analog voltage excitation of the prior art. Since the present invention incorporates certain elements of circuit 10, a detailed review of its operation will aid in understanding the teachings of the present invention.

The analog excitation voltage comprises a timed series of small voltage steps that are digitally generated beginning with counter 12 which is triggered by a precision clock which is not shown. The output of counter 12, which has 256 sequential digital values in this example, provides addresses for a LUT in RAM 14 in which are stored a plurality of digital data values representing the predetermined steps of a column excitation voltage waveform. Each digital data value has a resolution of 13 bits, i.e., 8192 possible values. These digital data values are sequentially provided to the input of a digital-to-analog converter (DAC) 16 which transforms them into discrete steps of an analog voltage that is applied to one or more of a plurality of column drivers 18.

This controlled excitation voltage provides the charging source for one or more of a plurality of columns 20 of the RLCD. In this example, 640 columns of the 1024 columns of the representative RLCD are supplied by a single column driver 18.

As the individual column voltage rises, a predetermined digital counter value corresponding to the termination time of that voltage rise is provided for each column by data buffer 22 as one input to digital comparator 24. When the identical output value from counter 12 is present at the other input of comparator 24, comparator 24 will cause the output of a column transfer gate 26 to latch closed, thereby halting the charge current to each column capacitance 28. The pixel is then displayed for the remainder of the frame time interval. Other columns will continue to charge until their unique predetermined values are reached, at which time they will be turned off and the pixels displayed for the remainder of the frame time.

At the end of the charge and display time, a flight back mode is entered, whereby a high current switching device will quickly discharge the column capacitance back to a predetermined reference level within approximately 50 nanoseconds. The currents in this device can approach two amperes during this discharge operation. A representative RLCD device would have a structure of 1280 columns and 1024 rows and have an on-panel integrated pixel switch located between a pixel capacitance and a column, the switch being controlled by a row voltage signal.

Figure 2 shows an exemplary embodiment of a control circuit 30 for an analog current excitation path of a plurality of RLCD columns 20 which is fabricated according to the present invention. Control circuit 30 generates excitation signals required to create an image on a high-resolution display, such as a 1280 row and 1024 column RLCD at 8 bits per color on a silicon die. At a 60 Hz refresh rate, each frame is approximately 5 milliseconds in duration which allows for three colors per frame and provides for a row activity duration of approximately five microseconds.

As in circuit 10, counter 12 is triggered by a precision clock which is not shown. The output of counter 12, which has 256 sequential digital values in this example, provides addresses into a LUT located within a RAM module 32. However, in circuit 30, unlike circuit 10, each one of the plurality of stored digital data values represents the time-derivative of the steps of a column excitation current waveform, with each value having a resolution of at most 8 bits, i.e., 256 possible values. Each one of the plurality of digital data values are sequentially provided to the input of an IDAC 34 which integrates the digital values and presents an analog output current to the input of a plurality of OTAs 36. Each one of the plurality of OTAs 36 is in series with a single column capacitance 28 of the RLCD.

As in circuit 10, when the column capacitance 28 of circuit 30 has charged to a predetermined value, the predetermined counter value in data buffer 22 is reached and each

one of the plurality of column comparators 24 will cause the output of each associated one of the plurality of column OTAs 36 to switch to the tri-state or high output impedance state, thereby halting the charge current to that column capacitance 28. The pixels are then displayed for the remainder of the frame time.

Other columns will continue to charge until their unique predetermined values are reached, at which time they will be switched to the tri-state mode. Although this high impedance state is incorporated within the architecture of an OTA 36, it is represented in circuit 30 as an open switch 38 for purposes of clarity. At the end of the charge and display time, a flight back mode is entered whereby an external high current MOS switching device quickly discharges the column capacitance back to a predetermined reference level within approximately 50 nanoseconds.

Since the digital comparator 24 tri-states the output of OTA 36 based on the comparison of an upstream digital signal from the output of counter 12 output rather than the actual voltage on the column capacitance 28, errors can arise at the outputs that need correction. To compensate for such errors, a low current feedback circuit which is not shown compares the actual resultant peak column voltage with a reference voltage for each color and provides an auto-scaling correction signal to control circuit 30 to provide minor adjustment to the column voltages. In addition, at the end of a line period, each column analog voltage value is sampled and stored for calibration use on the next cycle. Each respective value will provide the initial reference voltage for its corresponding column during the following frame.

Control circuit 30 uses small-chip-area circuitry which is more suited for implementation on a high density integrated circuit chip than the larger components used in conventional circuits having a voltage output. Moreover, by limiting the driver circuitry to only low current capability current sources, the noise feed-through to adjacent pixels that is associated with high current spikes is minimized.

Figure 3 shows representative waveforms for the voltage applied to the RLCD columns of circuit 30. The controlled low current provided by OTA 36 of circuit 30 is integrated by panel capacitance 28 to produce a controlled voltage rise in columns 20 and to avoid the generation of the noisy instantaneous current spikes. Waveform 40 represents a typical applied ramp voltage waveform that results from the charge current being applied to column capacitance 28 for the complete row time.

Waveform 42 shows the latching signal applied to the charging OTA 36, and waveform 44 illustrates the resulting envelope of the voltage on the column associated with

waveform 42. While waveform 42 is a constant amplitude current pulse, the actual waveform of the charging current applied can be any one of a variety of waveforms and is exclusively controlled by the LUT within RAM module 32. Auto-calibration occurs at location 46 on waveform 42 and column discharge occurs at location 48 on waveform 42.

Numerous modifications to the alternative embodiments of the present invention will be apparent to those skilled in the art in view of the foregoing description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention. Details of the structure may be varied substantially without departing from the spirit of the invention and the exclusive use of all modifications which come within the scope of the claims is reserved.

CLAIMS:

1. An image processing system for an RLCD comprising
a digital data generating means for generating digital values,
means for driving one or more of a plurality of vertical columns in response to the digital values,
an RLCD device comprised of a plurality of vertical columns and a plurality of horizontal rows,
an RLCD column selection means, and
RLCD row selection means,
a discharge means for returning the voltage on each one of a plurality of vertical columns to a reference voltage at the end of a row time and
a calibration means for adjusting color voltage levels, characterized in that the means for driving the one or more of a plurality of vertical columns comprises a plurality of integrating digital-to-analog converters providing analog current outputs in response to the digital values, the integrating digital-to-analog converter current output driving the one or more of a plurality of the vertical columns.

2. The image processing system according to claim 1, wherein the digital data generating means comprises:
a RAM (32) having a LUT for storing a plurality of time-derivative digital values corresponding to a different one of a plurality of current levels in the RLCD; and
a digital counter (12) for providing addresses to the RAM (32).

3. The image processing system according to claim 2, wherein the LUT is comprised of 256 digital values having at most a binary word length of 8 bits each.

4. The image processing system according to claim 2, wherein the LUT is comprised of 256 digital values having at most a binary word length of 6 bits each.

5. The image processing system according to claim 2, wherein a structure of the RLCD device is comprised of 1280 columns (20) and 1024 rows.

6. The image processing system according to claim 1, wherein the IDAC (34) output current drives one or more of a plurality of vertical RLCD columns (20) not exceeding 640.

7. The image processing system according to claim 1, wherein the column selection means is comprised of a plurality of OTAs (36), each separate one of the plurality of OTAs (36) being coupled in series with a separate one of the plurality of columns (20).

8. The image processing system according to claim 7, wherein OTA (36) conduction begins at the start of a row time period and ends in response to a latching input signal.

9. The image processing system according to claim 8, wherein the latch signal is generated as a result of a digital comparison between a digital counter (12) output value and a stored counter data value corresponding to a desired pixel voltage for a particular one of the plurality of columns (20).

10. The image processing system according to claim 1, wherein the column selection means causes the RLCD column voltage to monotonically increase in a controlled manner to a predetermined level through capacitive charging action of the applied current on the intrinsic column capacitance (28).

11. The image processing system according to claim 1, wherein the discharge means is an external MOS switch.

12. The image processing system according to claim 1, wherein the calibration means comprises:

an analog comparator for comparing a sampled column voltage with a predetermined reference voltage level; and

a correction means for adjusting and retaining said corrected column voltages.

13. An RLCD device comprising a row switch integrated at each different one of a plurality of pixel locations,

a matrix structure comprised of a plurality of vertical columns and a plurality of horizontal rows,

a column selecting means and

a row selecting means

characterized in that the columns selecting means is arranged for beginning and ending current flow to each different one of a plurality of columns in response to a logical input signal.

14. The RLCD device according to claim 13, wherein the matrix structure is comprised of 1280 columns (20) and 1024 rows.

15. The RLCD device according to claim 13, wherein the column selection means comprises an integrated OTA (36).

16. The RLCD device according to claim 13, wherein the row selection means comprises a digital input signal applied to the row switch.

17. A method for generating an image in an RLCD, comprising the steps of:

a) obtaining a first one of a plurality of digital values within a LUT;

b) time-integrating the digital value;

c) converting the digital value to an analog current value;

d) time-integrating the analog current value; and

e) repeating steps a-d for each other one of the plurality of digital values within the LUT until a predetermined terminating digital counter (12) value is attained.

18. The method according to claim 17, wherein the plurality of digital values stored within the LUT are the time-derivative values of the plurality of current values required to create a monotonically increasing voltage ramp when integrated with the intrinsic column capacitance (28) of the RLCD.

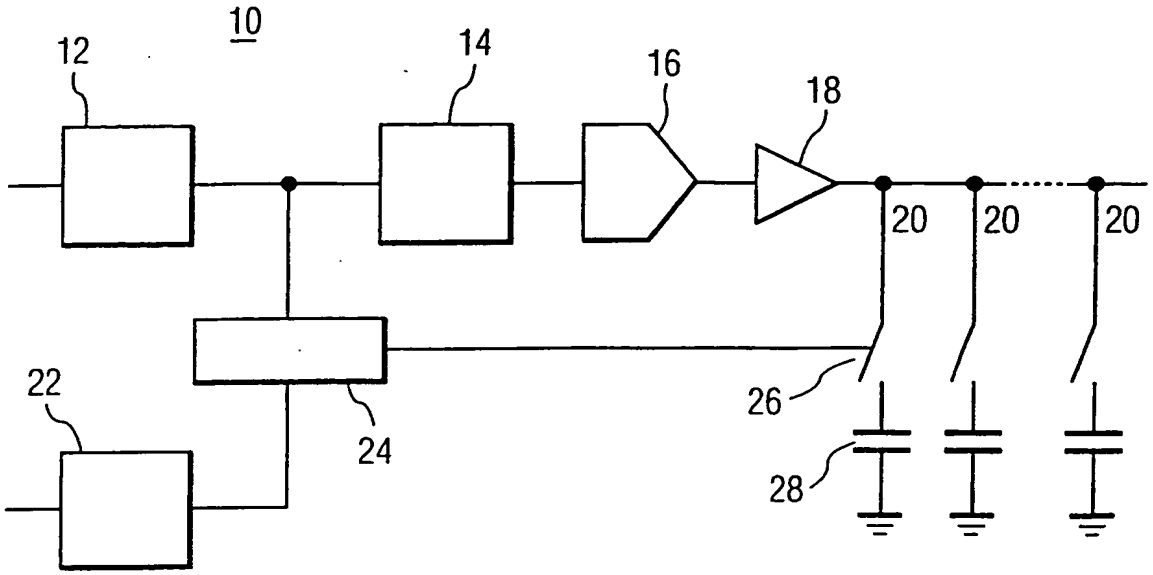
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FIG. 1

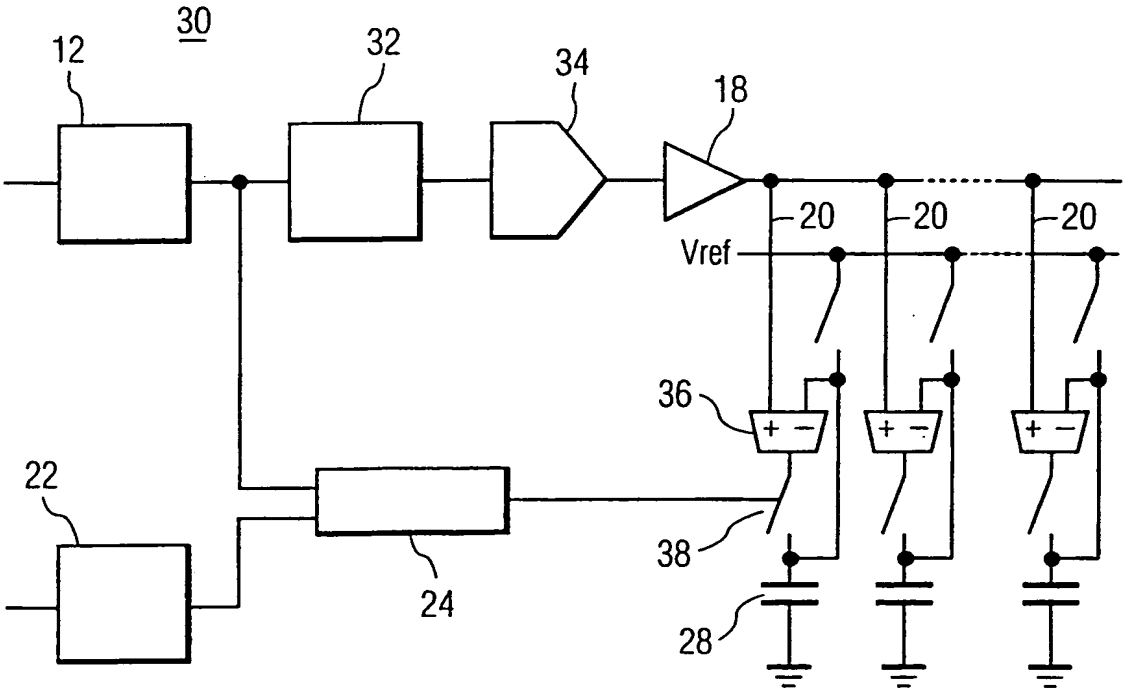
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FIG. 2

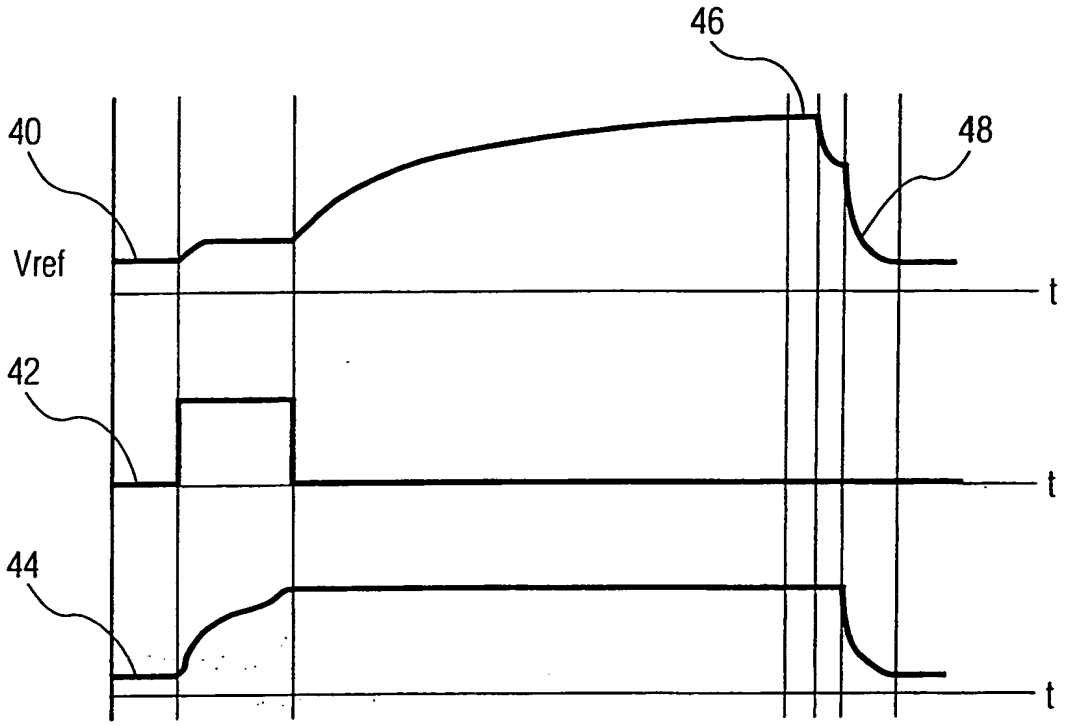

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 01/02998

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 006 739 A (KABUTO NOBUAKI ET AL) 9 April 1991 (1991-04-09) column 3, line 30 -column 4, line 14; figure 3	13,14,16
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 047 (P-1162), 5 February 1991 (1991-02-05) & JP 02 281291 A (SEIKO EPSON CORP), 16 November 1990 (1990-11-16) abstract	13,14,16
A	US 4 353 062 A (LORTEIJE JEAN H J ET AL) 5 October 1982 (1982-10-05) column 7, line 55 -column 9, line 10	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/EP 01/02998

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